What is claimed is:

1. A method for detecting faults in connections which connect a first module and a second module, following an event initiating the detection method, determining one of the modules as initiator and one of the modules as responder, comprising:

sending the initiator, in a first step, a first value and sending a second value, in a second step, to the responder over a connection, wherein a first sequence and the first and second value are known to the responder as a first expected sequence;

checking, via the responder, whether the values received in the first and second step match the first expected sequence;

if the check by the responder is successful, in a third step, sending, via the responder, a third value and, in a fourth step, sending a fourth value to the initiator over the connection, wherein a second sequence and the third and fourth value are known to the initiator as a second expected sequence;

if the check by the responder is a negative outcome, in the third step, sending, via the responder, the fourth value and, in the fourth step, sending the third value to the initiator over the connection and marking the connection as faulty;

checking, via the initiator, whether the values received in the third and fourth step match the second expected sequence;

if the check by the initiator is successful, sending, in a fifth step, via the initiator, a fifth value and, in a sixth step, sending a sixth value to the responder over the connection, wherein a third sequence and the fifth and sixth value are known to the responder as a third expected sequence;

if the check by the initiator is a negative outcome, sending, in the fifth step, via the initiator, the sixth value and, in the sixth step, sending the fifth value to the responder over the connection and marking the connection as faulty;

checking, via the responder, whether the values received in the fifth and sixth step match the third expected sequence, and marking the connection as faulty if the check has a negative outcome.

2. The method as claimed in claim 1, wherein the first and second, third and fourth, and fifth and sixth values are pair-wise different in each case.

3. The method as claimed in claim 1, wherein the first and the second step are repeated at least once after completion of the second step, with the first expected sequence being extended accordingly,

the third and the fourth step are repeated at least once after completion of the fourth step, with the second expected sequence being extended accordingly, and

the fifth and the sixth step are repeated at least once following the sixth step, with the third expected sequence being extended accordingly.

4. The method as claimed in claim 1, wherein one of the modules is determined as initiator and one of the modules is determined as responder by at least on of means of static, administrative definition, by mounting location-dependent definition, by a signal via a separate connection of the modules, and by a signal by means of a protocol over existing connections of the modules.

5. The method as claimed in claim 1, wherein an existing fallback connection is activated for a connection marked as faulty by a control logic device which controls the detection method.

6. The method as claimed in claim 1, wherein for detecting faults on binary connections, one of the values 0 or 1 is selected for the first, the third and the fifth value in each case, and the second value is obtained from logical inversion of the first value, the fourth value is obtained from logical inversion of the third value, and the sixth value is obtained from logical inversion of the fifth value.

7. The method as claimed in claim 6, wherein for bus connections having a width of n bits, which are formed by n binary connections, the detection method is performed for each of the n binary connections.

8. The method as claimed in claim 7, wherein for the bus connections having a width of n bits, which are formed by the n binary connections, at least one binary fallback connection is provided which is activated if one of the n binary connections is marked as faulty.

9. A method for correcting faults in connections between digital modules, comprising:

forming a connection by a first group of active connection lines and providing a second group of inactive connection lines accordingly; and

activating an inactive connection line of the second group and deactivating a connection line that has been active up until this point if the active connection line is found to be faulty by the control logic device,

wherein the control logic device in cooperation with a multiplexing device controls activation and deactivation.

10. A circuit arrangement for correcting faults on connections between digital modules, comprising:

a control logic device to detect arrangement-internal and arrangement-external faults of input/output connections and a multiplexer device to switch over data

transmission of faulty active input/output connections to fault-free inactive input/output connections.

11. The circuit arrangement as claimed in claim 10, wherein the control logic device has a unit which performs: sending an initiator, in a first step, a first value and sending a second value, in a second step, to a responder over a connection, wherein a first sequence and the first and second value are known to the responder as a first expected sequence;

checking, via the responder, whether the values received in the first and second step match the first expected sequence;

if the check by the responder is successful, in a third step, sending, via the responder, a third value and, in a fourth step, sending a fourth value to the initiator over the connection, wherein a second sequence and the third and fourth value are known to the initiator as a second expected sequence;

if the check by the responder is a negative outcome, in the third step, sending, via the responder, the fourth value and, in the fourth step, sending the third value to the initiator over the connection and marking the connection as faulty;

checking, via the initiator, whether the values received in the third and fourth step match the second expected sequence;

if the check by the initiator is successful, sending, in a fifth step, via the initiator, a fifth value and, in a sixth step, sending a sixth value to the responder over the connection, wherein a third sequence and the fifth and sixth value are known to the responder as a third expected sequence;

if the check by the initiator is a negative outcome, sending, in the fifth step, via the initiator, the sixth value and, in the sixth step, sending the fifth value to

the responder over the connection and marking the connection as faulty;

checking, via the responder, whether the values received in the fifth and sixth step match the third expected sequence, and marking the connection as faulty if the check has a negative outcome.

12. The circuit arrangement as claimed in claim 10, wherein

the circuit arrangement is part of an integrated circuit.